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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/692,647	10/19/2000	Martin McAfee	016295.0620 (DC-02500)	8276

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EXAMINER	
BADERMAN, SCOTT T	

ART UNIT	PAPER NUMBER
2113	9

DATE MAILED: 05/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/692,647	MCAFEE, MARTIN	
	Examiner	Art Unit	
	Scott T Baderman	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 17-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 17-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 and 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (hereinafter "AAPA") in view of Drucker (5,591,984).

As in claim 1, AAPA discloses a debugging circuit capable of debugging a plurality of microprocessor sockets and any respective microprocessors included therein that comprises a debug port and a plurality of microprocessor sockets, wherein each of the microprocessor sockets are adapted to receive a microprocessor, and wherein the plurality of microprocessor sockets are adapted to form a serial signal path (see pp. 1-3 of the specification). Although AAPA discloses termination capabilities built into the CPU to ensure termination (see p. 2), AAPA does not disclose a plurality of switches, wherein each of the switches correspond to a respective one of the plurality of microprocessor sockets, and wherein each of the switches is capable of automatically detecting whether a microprocessor is present in the corresponding microprocessor socket, and if a microprocessor is present, then the switch is automatically configured to include the microprocessor within the signal path, and if the microprocessor is not present, then the

switch is automatically configured so that the signal path bypasses the corresponding microprocessor socket. Drucker discloses a system that comprises a plurality of sockets (slots) adapted to receive a respective one of a plurality of plug-in modules (microprocessors) and a plurality of switches, wherein each of the switches correspond to a respective one of the plurality of microprocessor sockets, and wherein each of the switches is capable of automatically detecting whether a microprocessor is present in the corresponding microprocessor socket, and if a microprocessor is present, then the switch is automatically configured to include the microprocessor within the signal path, and if the microprocessor is not present, then the switch is automatically configured so that the signal path bypasses the corresponding microprocessor socket (see entire patent).

It would have been obvious to a person skilled in the art at the time the invention was made to implement the system taught by Drucker above into the system taught by AAPA above. This would have been obvious because both systems respectively teach of circuits that include a plurality of microprocessor sockets connected along a signal path, and which are adapted to receive a microprocessor. Further, Drucker clearly teaches that since a given slot may or may not hold a module, some means must be provided for bypassing the signal around an empty slot and passing the signal through the slot when a module is present therein (column 1: lines 20-24). Drucker further teaches that it is known to provide the selective bypass function by using manual or mechanical jumpering schemes, however, such schemes have proven to be unreliable (column 1: lines 27-29).

As in claim 2, AAPA clearly teaches wherein a debugging input is provided to each microprocessor socket, and wherein a debugging output is provided from each microprocessor that is present in the corresponding microprocessor socket (see p. 2, lines 12-14 of the specification).

As in claim 3, Drucker discloses wherein each switch receives as an input a microprocessor detection signal (via current sensing) indicating whether the corresponding microprocessor is present (Figure 1, column 1: lines 46-55).

As in claim 4, Drucker discloses that for each switch, if the microprocessor is present, then the switch allows the signal to pass through the slot (Figure 1, column 1: lines 20-24 and 46-55), and AAPA discloses that when the microprocessor is present the microprocessor will provide a debugging output (see pp. 1-2 of the specification).

As in claim 5, Drucker discloses that for each switch, if the microprocessor is not present, then the switch provides that the signal bypasses the empty slot (Figure 1, column 1: lines 20-24 and 46-55).

As in claim 6, Drucker discloses that for each switch not corresponding to a last slot in the signal path, the switch allows the signal to pass through or bypass the slot (Figure 1, column 1: lines 20-24 and 46-55), and AAPA discloses that when the microprocessor or terminator card

is present, the microprocessor or terminator card will provide a signal to the subsequent microprocessor (see pp. 1-2 of the specification).

As in claim 7, it is implied that there will eventually be a last slot in the signal path taught by Drucker. Further, AAPA discloses that the signal passes through each successive microprocessor before returning to the debugging computer through the debug port (see p.2 of the specification).

As in claim 8, AAPA discloses wherein the debug port is electrically coupled to a computer and receives input from and provides output to the computer (see pp. 1-2 of the specification).

As in claims 9 and 10, Drucker discloses wherein the plurality of switches each comprise a pair of bipolar transistors or field effect transistors (Figures 2-4, column 3: lines 16-61).

As in claim 17, the Applicant is directed to claims 1, 3, 4 and 6 above.

As in claim 18, the Applicant is directed to claim 6 above.

As in claim 19, the Applicant is directed to claim 7 above.

As in claim 20, the Applicant is directed to claims 1 and 8 above.

As in claims 21 and 22, the Applicant is directed to claims 9 and 10 above.

Response to Arguments

3. Applicant's arguments with respect to claims 1-10 and 17-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott T Baderman whose telephone number is (703) 305-4644. The examiner can normally be reached on Monday-Friday, 6:45 AM-4:15 PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Scott T Baderman
Primary Examiner
Art Unit 2113

STB